In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A digital processing system having a microprocessor, wherein the microprocessor comprises:

fetch circuitry for fetching instruction fetch packets from sequential memory address locations, wherein each fetch packet contains a first plurality of fixed and equal length instructions, each instruction including an instruction type and a predetermined p-bit, said p-bit having a first digital state indicating a next instruction is to execute in parallel with said instruction and a second digital state indicating a next instruction is to execute in a cycle after said instruction;

a second plurality of functional units, each of the second plurality of functional units operable to execute a corresponding instruction in parallel with other functional units, and

dispatch circuitry connected to said fetch circuitry and said second plurality of functional units operable to

select an execute packet from two fetch packets, wherein an execute packet varies in size and contains only a set of instructions that can be executed in parallel on the plurality of functional units, by scanning instructions from lower memory address locations to higher memory address locations beginning in a first fetch packet, adding an instruction to said execute packet when said p-bit of a prior instruction has said first digital state and continuing past an end of said first fetch packet to a beginning of a second fetch packet until said p-bit of an instruction has said second digital state, and

dispatch each instruction of said selected execute packet to a functional unit corresponding to said instruction type of said instruction,

wherein the dispatch circuitry comprises:

a first latch to hold said first plurality of instructions of a first fetch packet, said first latch including a first plurality of sections, each section storing a corresponding one of said first plurality of instructions of said first fetch packet;

a second latch to hold said first plurality of instructions of a second fetch packet immediately following said first fetch packet, said second latch including a first plurality of sections, each section storing a corresponding one of said first plurality of instructions of said second fetch packet;

a first plurality of multiplexers, each multiplexer having exactly two data inputs, a first data input receiving an entire instruction from a predetermined section of said first latch and a second data input receiving an entire instruction from a corresponding section of said second latch, a control input and an output, each multiplexer selecting at said output either said entire instruction from said section of said first latch, said entire instruction from said section of said second latch, or no instruction, dependent upon said control input;

a dispatch control circuit connected to said first latch, said second latch, and said plurality of multiplexers, said dispatch control circuit receiving said predetermined p-bit from each instruction of said first latch and each instruction of said second latch for control of said plurality of multiplexers via said control inputs according to the execute packets determined by only said p-bits; and

a cross point circuitry connected to said outputs of said plurality of multiplexers for dispatching said instructions at said output of said multiplexers to a functional unit corresponding to said instruction type of each instruction.

Claims 2 to 6 (Canceled)

7. (Currently Amended) A method of operating a digital system having a microprocessor, wherein the microprocessor has a plurality of functional units for executing instructions in parallel, comprising the steps of:

storing fixed and equal length instructions at sequential memory address locations, each instruction including an instruction type and a predetermined p-bit, said p-bit having a first digital state indicating a next instruction is to execute in parallel with said instruction and a second digital state indicating a next instruction is to execute in a cycle after said instruction;

fetching a sequence of instruction fetch packets, wherein each fetch packet contains a first plurality of instructions;

scanning the p-bit of each instruction of each fetch packet from lowest memory address location in a first memory fetch packet to highest memory address location in a second immediately following fetch packet to determine an execute packet dependent on the p-bits, wherein said step of determining an execute packet boundary dependent upon the p-bits includes

storing each instruction of said first fetch packet in a corresponding section of a first latch,

storing each instruction of said second fetch packet in a corresponding section a second latch, and

selecting only either an entire instruction from a predetermined section of said first latch, an entire instruction from a corresponding section of said second latch,

or no instruction, dependent upon only said p-bit from each instruction stored in said first latch and each instruction stored in said second latch; and

dispatching each instruction within the determined execute packet to one of a second plurality of execution units dependent upon an instruction type of the instruction.

Claims 8 to 11. (Canceled)